

## Evaluating the LTC9111, IEEE 802.3cg SPoE PD Controller

### FEATURES

- ▶ IEEE 802.3cg-compliant SPoE PD
- ▶ Supports serial communication classification protocol (SCCP)

### ONLINE RESOURCES

- ▶ [Schematic, PCB layout, and bill of materials](#)

### GENERAL DESCRIPTION

The EVAL-LTC9111-AZ is an evaluation motherboard featuring the LTC9111, an IEEE 802.3cg-compliant single pair power over Ethernet (SPoE) powered device (PD) controller.

With the LTC9111 wide operating range of 2.3V to 60V, the EVAL-LTC9111-AZ may be configured with class jumpers to IEEE 802.3cg 24V power classes (Class 10 to Class 12) or 52V power classes (Class 13 to Class 15).

The EVAL-LTC9111-AZ motherboard headers (J1, J2, and J3) connect to SPoE shields, the [EVAL-10BT1L-MCS-AZ](#) (Class 10 to Class 14) or the [EVAL-10BT1L-MCS-BZ](#) (Class 15). The EVAL-LTC9111-AZ motherboard with a shield connects via a single pair Ethernet (SPE) cable to an IEEE 802.3cg SPoE power sourcing equipment (PSE) for power.

The EVAL-LTC9111-AZ incorporates both IEEE 802.3cg-compliant wakeup signature and SCCP-based classification.

### EVALUATION BOARD PHOTOGRAPH

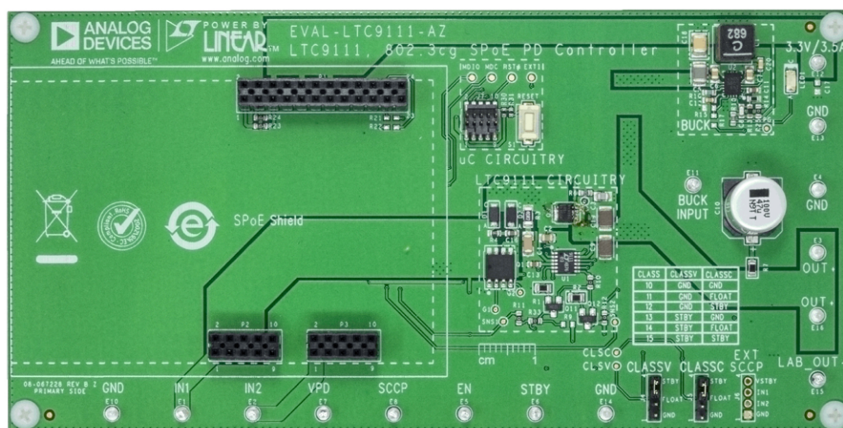


Figure 1. EVAL-LTC9111-AZ Evaluation Board Photograph

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REVISION HISTORY

7/2025—Revision 0: Initial Version



EVALUATION BOARD QUICK START PROCEDURE

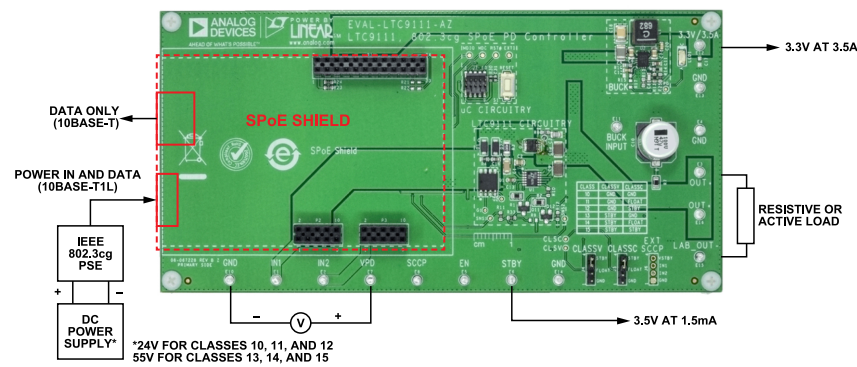


Figure 3. Setup Diagram for the EVAL-LTC9111-AZ with Resistive or Active Load

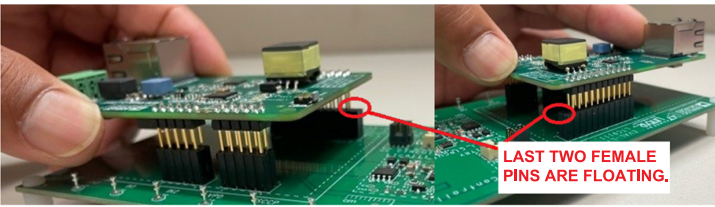


Figure 4. Alignment of SPoE Shield with the EVAL-LTC9111-AZ

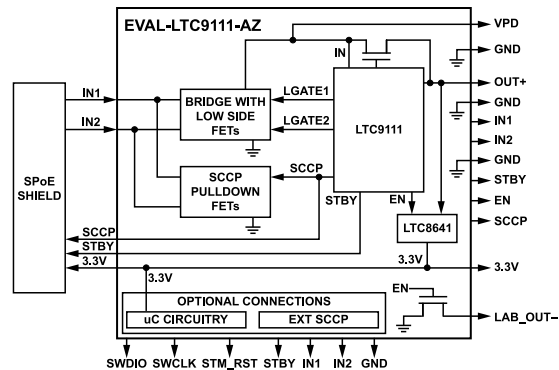


Figure 5. Block Diagram Showing Signal Connections for the EVAL-LTC9111-AZ

## EVAL-LTC9111-AZ DEMONSTRATION CIRCUIT

## SHIELD INSTALLATION

The EVAL-LTC9111-AZ PD motherboard can accept one media converter shield. For Class 10 to Class 14 evaluations, install the [EVAL-10BT1L-SMC-AZ](#). For Class 15 evaluation, install the [EVAL-10BT1L-SMC-BZ](#).

When inserting a shield on to the motherboard, align the two short male headers of the shield with the two short female headers at a port on the motherboard (see [Figure 4](#)). The longer header naturally aligns. The last two pins of the longer header on the motherboard are reserved for future use and do not have pins inserted in them. Insert the shield until the headers are flush with each other. Before proceeding, verify no pins are sticking out indicating a misalignment.

Note that powering the EVAL-LTC9111-AZ motherboard with a misaligned shield can cause damage to the system.

## INPUT POLARITY CORRECTION

IEEE 802.3cg requires input polarity insensitive PDs to facilitate fool-proof field installation with screw terminals. The EVAL-LTC9111-AZ PD motherboard polarity corrects the two inputs, IN1 and IN2. The [LTC9111](#) drives external MOSFETs for the low-side rectifiers and relies on external Schottky diodes for the high-side rectifiers. Active low-side rectification minimizes power losses and overcomes circuit start-up challenges posed by the constraints in the standard. Footprints for both dual-MOSFET (single package, default option) at Q1, and discrete 3mm × 3mm DFN MOSFETs at Q2 and Q4 (optional), are available on the PCB for the active low-side rectifiers.

## SPOE PD CLASS

The LTC9111 SPoE PD class is configured by the CLASSC and CLASSV pins. CLASSV is a binary input, either low by connecting to GND or high by connecting to STBY. CLASSV is tied low for the 24V classes (Class 10 to Class 12), and high for the 54V classes (Class 13 to Class 15). CLASSC is a trinary input, set either low by connecting to GND, high by connecting to STBY, or high impedance by floating the pin. Refer to [Table 1](#) for configuration options and [Figure 6](#) for jumper location.

CLASS	CLASSV	CLASSC
10	GND	GND
11	GND	Float
12	GND	STBY
13	STBY	GND
14	STBY	Float
15	STBY	STBY

Figure 6. EVAL-LTC9111-AZ CLASSC and CLASSV Jumpers

## OVERVOLTAGE PROTECTION FOR 24V PDS

When the LTC9111 is configured for Class 10 to Class 12 (that is, CLASSV pin is tied low), an overvoltage protection feature is enabled to protect downstream elements in the application from exposure to excessive voltage. When the input voltage exceeds  $V_{OV}$  (38.5, typ), the gate of the external hot swap MOSFET turns off, regardless of the port state.

## SENSE SNUBBER

A snubber between the SNS pins prevents high-frequency ringing when the rectifying diodes are reverse biased during SCCP logic transitions. On the EVAL-LTC9111-AZ motherboard, the P4 jumper connects or disconnects the sense snubber. Set the P4 jumper to CONNECT when using the EVAL-10BT1L-MCS-AZ SPoE shield (Class 10 to Class 14) to connect the sense snubber. Set the P4 jumper to DISCONNECT when using the EVAL-10BT1L-MCS-BZ SPoE shield (Class 15) as the sense snubber is already present on this SPoE shield. Refer to [Figure 7](#) for jumper location.

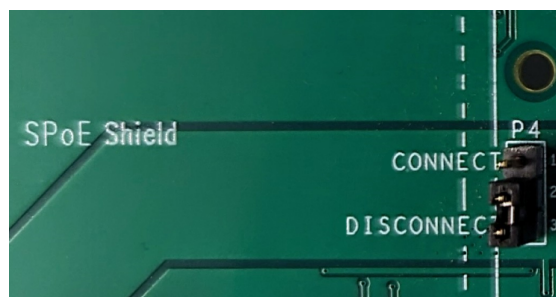


Figure 7. EVAL-LTC9111-AZ RC Snubber Jumper

## EVAL-LTC9111-AZ DEMONSTRATION CIRCUIT

### STBY SUPPLY

An internal linear regulator produces a nominal 3.5V supply at the STBY pin. It is used to power internal control circuitry. The STBY pin has a capacitance of 2.2 $\mu$ F placed near the pin.

Note that any external load on the STBY pin during classification may discharge the capacitor and cause brownout. There must be no load on the STBY pin during classification.

### ON-BOARD MICROCONTROLLER FOR PHY

The EVAL-LTC9111-AZ PD motherboard includes an on-board microcontroller for configuring an Ethernet PHY located on the SPoE shields via the MDIO interface.

Note that the microcontroller is not required for the [LTC9111](#) operation.

The microcontroller is powered from the on-board 3.3V buck regulator and the MDIO interface is isolated on the SPoE shield. Header J7 is used for programming the microcontroller. Switch S1 is used for resetting the microcontroller.

### ON-BOARD 3.3V BUCK REGULATOR

The EVAL-LTC9111-AZ PD motherboard has an on-board buck converter that steps the LTC9111 output down to a 3.3V logic rail. This supply powers the SPoE shield and on-board microcontroller. An additional 3.5A load may be connected to the 3.3V/3.5A turret. Refer to [Figure 8](#) for on-board 3.3V buck regulator location.

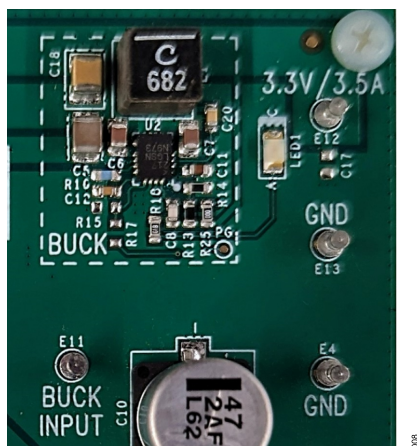


Figure 8. EVAL-LTC9111-AZ On-Board 3.3V Buck Regulator

### EXTERNAL SCCP HEADER

An external SCCP circuit may optionally perform classification instead of the LTC9111. The EXT SCCP header (J6) brings out the IN1 and IN2 inputs, as well as the STBY supply and GND. The external SCCP classification circuit may pull IN1 and IN2 to GND. The LTC9111 SCCP pull-down FETs (Q11 and Q12) must be disabled or uninstalled to not interfere with the external SCCP circuit. Refer to the [LTC4296-1](#) SCCP Wiki for more information on the classification protocol.

### LAB\_OUT CIRCUIT

During inrush, there can be significant transient power dissipation in the external MOSFET. Any load present before inrush is complete increases MOSFET stresses. LAB\_OUT- turret is a return path for resistive or active loads that are only connected after inrush has completed. The EN pin is held low then rises to 3.4V (typ) after inrush has completed. When EN is high, the LAB\_OUT circuit applies 12V to a power MOSFET gate which connects LAB\_OUT- to GND. Connect a resistive or active load between OUT+ and LAB\_OUT-.

Note that the user must not capacitively load LAB\_OUT-.

### OPTIONAL HOTSWAP MOSFET PACKAGE

Q13 provides an optional SOT-223 package footprint for the Hotswap MOSFET.

## NOTES

**ESD Caution**

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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